EXHIBIT M

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case No. IPR2022-00711
Patent No. 10,860,506

PATENT OWNER PRELIMINARY RESPONSE

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signal lines connecting the memory controller 12 and the DIMM 11 to each other are formed in the same length, the formula for calculating the second delay time Dt2 is simplified and the second delay time Dt2 for the data signal DQ input from the SDRAM during the read operation can be easily obtained. *Id*., 19:8-13.

VII. THE PETITIONER FAILED TO ESTABLISH A REASONABLE LIKELIHOD OF SUCCESS ON GROUND 1

Ground 1 relies on Hiraishi alone or, in the alternative, a combination of Hiraishi and Butt. In either case, the Petition is facially deficient and does not establish a reasonable likelihood of prevailing with respect to any claim of the '506 patent.

First, and as explained in more detail below, the Petitioner fails to present competent *prima facie* evidence that Hiraishi alone or in combination with Butt discloses each of the claim elements of at least independent claims 1 and 14.

Second, concerning the combination of Hiraishi and Butt, Petitioner wholly fails to explain why a POSITA would have been motivated, without the benefit of hindsight, to combine the references to create the claimed invention. Petitioner relies entirely on conclusory statements, lacking any explanation as to how the modifications would be carried out, much less why a POSITA would have perceived the benefits of such changes to outweigh the drawbacks. *See In re Van Os*, 844 F.3d 1359, 1362 (Fed. Cir. 2017) (stating that "a combination of prior art would have been . . . 'intuitive' is no different than merely stating the combination 'would have

been obvious'"); *Arctic Cat Inc. v. Polaris Indus., Inc.*, 795 F. App'x. 827 (Fed. Cir. 2019) ("The Board must weigh the benefits and drawbacks of the modification against each other, to determine whether there would be a motivation to combine.") (citing *Winner Int'l. Royalty Corp. v. Wang*, 202 F.3d 1340, 1349 n.8 (2000)).

A. Petitioner Failed to Establish That Hiraishi (Alone or With Butt) Discloses a Read Strobe That Is Delayed Based on Signals Received by the Data Buffer During a Previous Operation

Petitioner has not made a *prima facie* case that Hiraishi discloses a "first data buffer … configurable to, in response to one or more of the module control signals: delay the first read strobe by a first predetermined amount to generate a first delayed read strobe," where "the first predetermined amount is determined based at least on signals received by the first data buffer during one or more previous operations," as required by independent claim 1 (referred to herein as the "strobe delay feature"). The same deficiency exists with respect to the method of claim 14, which also recites the strobe delay feature as follows: "delaying the first read strobe by a first predetermined amount to generate a first delayed read strobe," and "before receiving the input C/A signals corresponding to the memory read operation at the module

control device, determining the first predetermined amount based at least on signals received by the first data buffer."[1]

Petitioner equates the strobe signal provided by Hiraishi's delay circuit 372 with the claimed "first delayed read strobe" and the delay of "about 90 degrees" with the claimed "first predetermined amount" of delay. *See* Petition, 35. Specifically, Petitioner contends that:

> Hiraishi's reference to circuit 372 delaying by "about 90 degrees" is qualified by "about" to allow for fine timing adjustments to the DQS signals by read leveling circuit 323, which would be calculated through a read leveling operation, e.g., step S4, "to adjust…a read timing in consideration of a propagation time of a signal.

Petition, 40 (citation omitted).

But, Hiraishi describes delaying the DQS signal by a fixed 90 degrees (1/4 clock cycle) by delay circuit 372, relative to the input DQS 351 or 352, where the DQS can be used as "an input trigger signal" for the FIFO (Read) circuit 302. EX1005 (Hiraishi), [0091]. There is simply no teaching or suggestion in Hiraishi that delay circuit 372 performs any "fine timing adjustments to the DQS signals by

[1] Claims 15-17 depend, either directly or indirectly, on independent claim 14 and further recite a predetermined amounts of delay "determined based on signals received by the second data buffer during one or more previous operations."

read leveling circuit 323," as alleged. Nor does Petitioner point to any specific signal from the read leveling circuit 323 that is inputted to the delay circuit 372 to effect this alleged fine adjustment.

To institute on this basis requires that the Board adopt a standard *for prima facie* evidence that requires nothing more than quoting vague language from a reference without any competent evidence as to what it means or discloses to a POSITA.

As Petitioner acknowledges, Hiraishi describes that this fixed "about" 90 degree delay is applied by delay circuit 372 in the case of a read operation. *See* EX1005, [0091] ("A phase of the selected data strobe signal DQS is delayed by about 90 degrees by a delay circuit 372, and then the data strobe signal DQS is supplied to the FIFO (Read) circuit 302 as an input trigger signal."); Petition, 40. Moreover, the only input to delay circuit 372 is a DQS signal (either from L1 or L2 based on selector 332). *See* EX1005, [0091] ("[T]he selector 332 selects a data strobe signal DQS input from either one of the input/output terminals 351 and 352. A phase of the selected data strobe signal DQS is delayed by about 90 degrees by a delay circuit 372, and then the data strobe signal DQS is supplied to the FIFO (Read) circuit 302 as an input trigger signal."); Decl., ¶100. In other words, delay circuit 372 is a circuit that is not disclosed as connected to any circuitry capable of providing any input that could alter the amount of delay applied by circuit 372 to the DQS

establish a reasonable likelihood of prevailing as to any claim, and therefore cannot form a basis for institution.

X. CONCLUSION

Based on the foregoing, the Board should deny the Petition in its entirety and decline to institute a *inter partes* review of the '506 patent.

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Respectfully submitted,

By: */Jonathan M. Lindsay/*

H. Annita Zhong (Reg. No. 65,530)
Jonathan M. Lindsay (Reg. No. 45,810)
Jason Sheasby (*pro hac vice* to be requested)
Irell & Manella LLP
1800 Avenue of the Stars, Suite #900
Los Angeles, CA 90067-4276
Telephone: (310) 203-7183
Fax: (310) 203-7199

Attorney for Patent Owner
Netlist, Inc.